Total Dose and Single Event Effects Testing of a Commercial 0.8µm CMOS Gate Array Process

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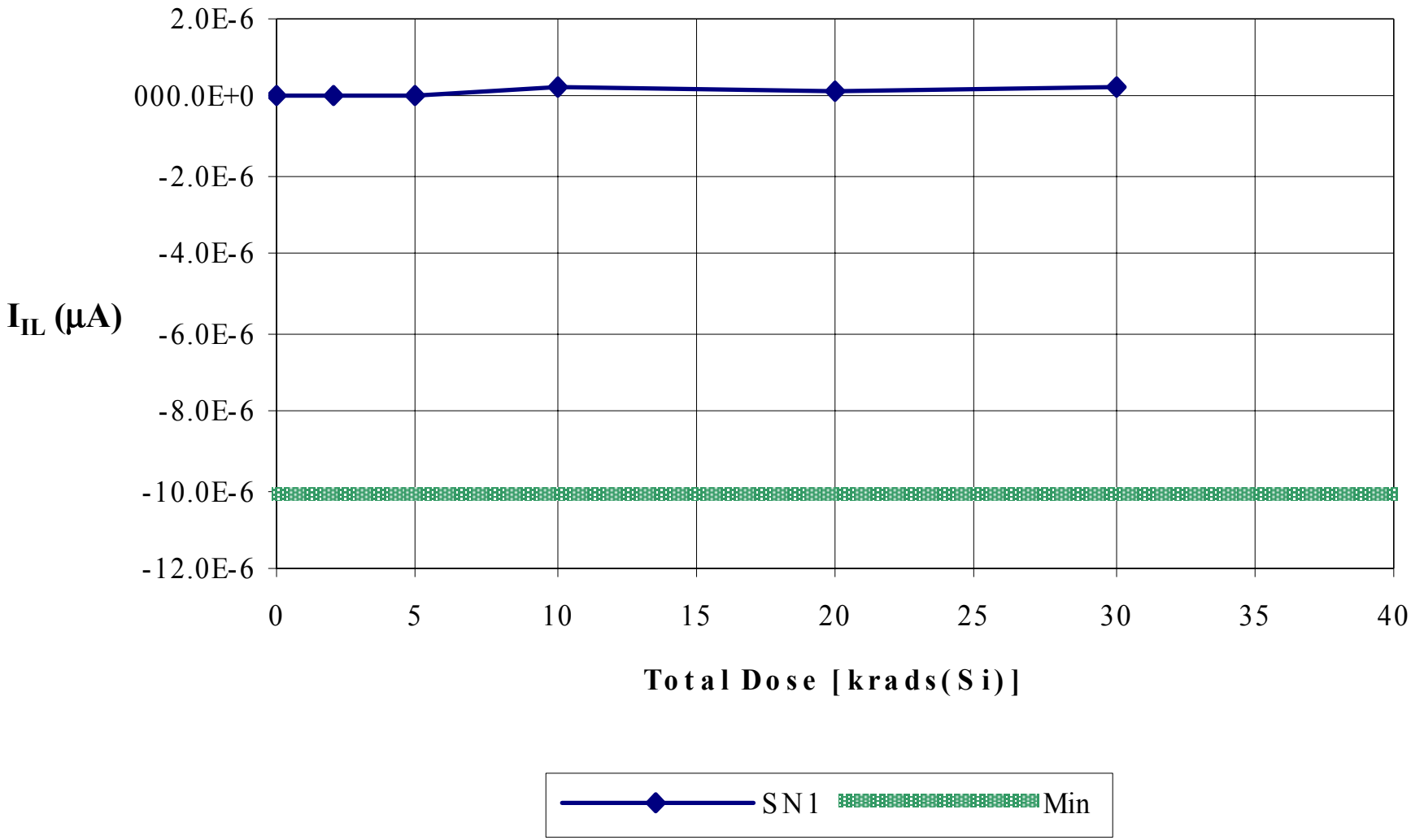
Abstract

Results are reported from total dose and Single Event Effects (SEE) testing of a Space Electronics, Inc. (SEi) low cost, high performance commercial SF6 0.8µm CMOS gate array process. Intrinsic total dose levels are demonstrated for up to 25 krad(Si). No Single Event Upsets (SEU) were detected in the combinatorial logic gates. Onsets of flip-flop errors were observed at LET_{TH} ~ 26 MeV/mg/cm^2 with a saturated cross section of 1.7 x 10^{-6} cm^2/bit. No Single Event Latchup (SEL) or loss of functionality was observed.

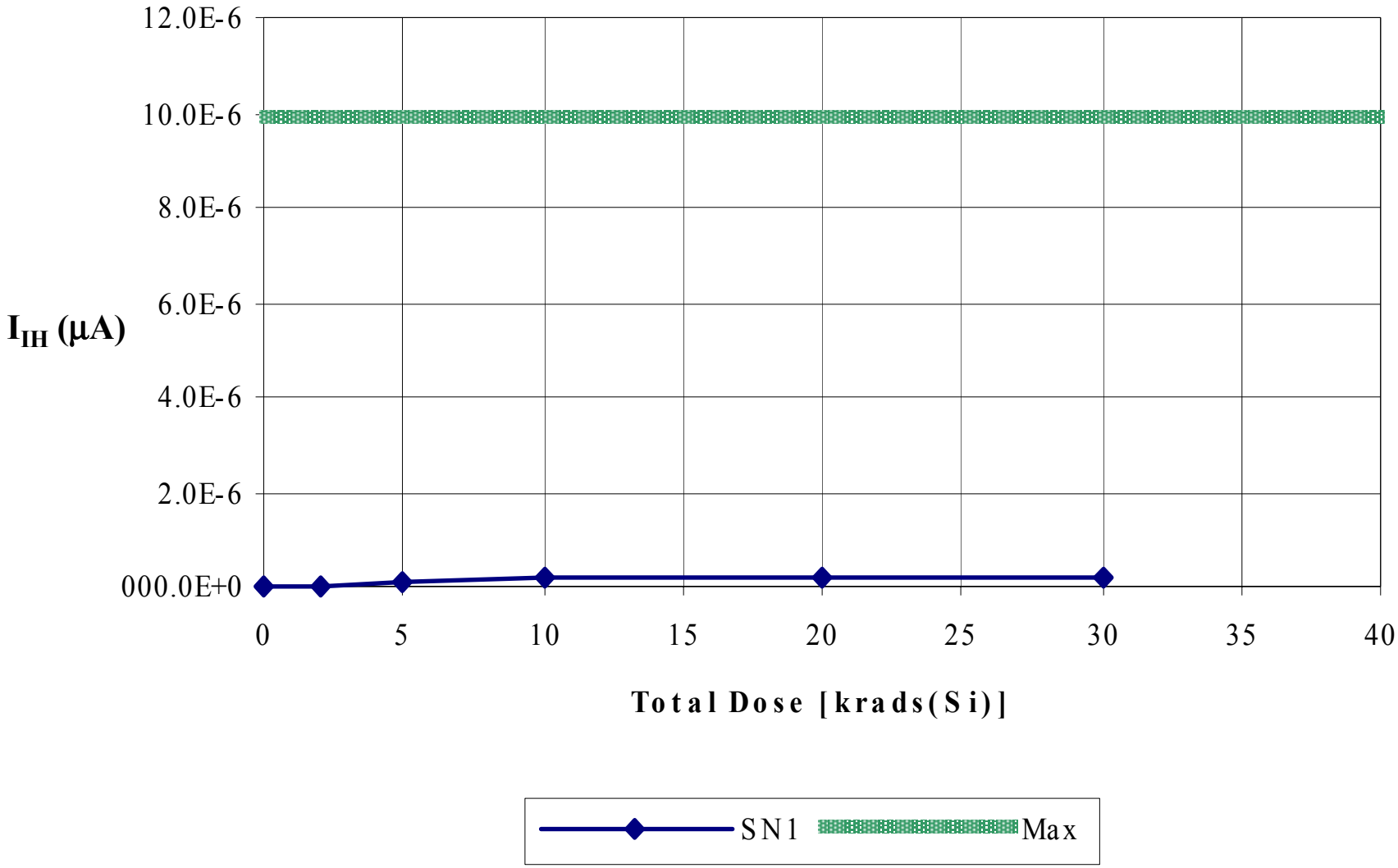
Introduction

Application Specific Integrated Circuits (ASICs) from commercial wafer foundries offer performance, cost, and time-to-market advantages for both commercial and military satellite programs when compared to dedicated rad-hard foundries. However, these commercial ASICs cannot meet many of today's space system requirements for total dose hardness, SEU immunity, or SEL immunity. Through a partnership with a ISO 9001 certified wafer foundry, SEi's SF6 family of radiation-hardened gate arrays are being fabricated on a commercial 0.8µm CMOS process. Built on epitaxial substrate wafers, the SF6 gate arrays combine SEi's digital Space Environment Modular Design (SEMD™) methodology with RAD-PAK® packaging technology to produce radiation-hardened ASICs suitable for space applications.

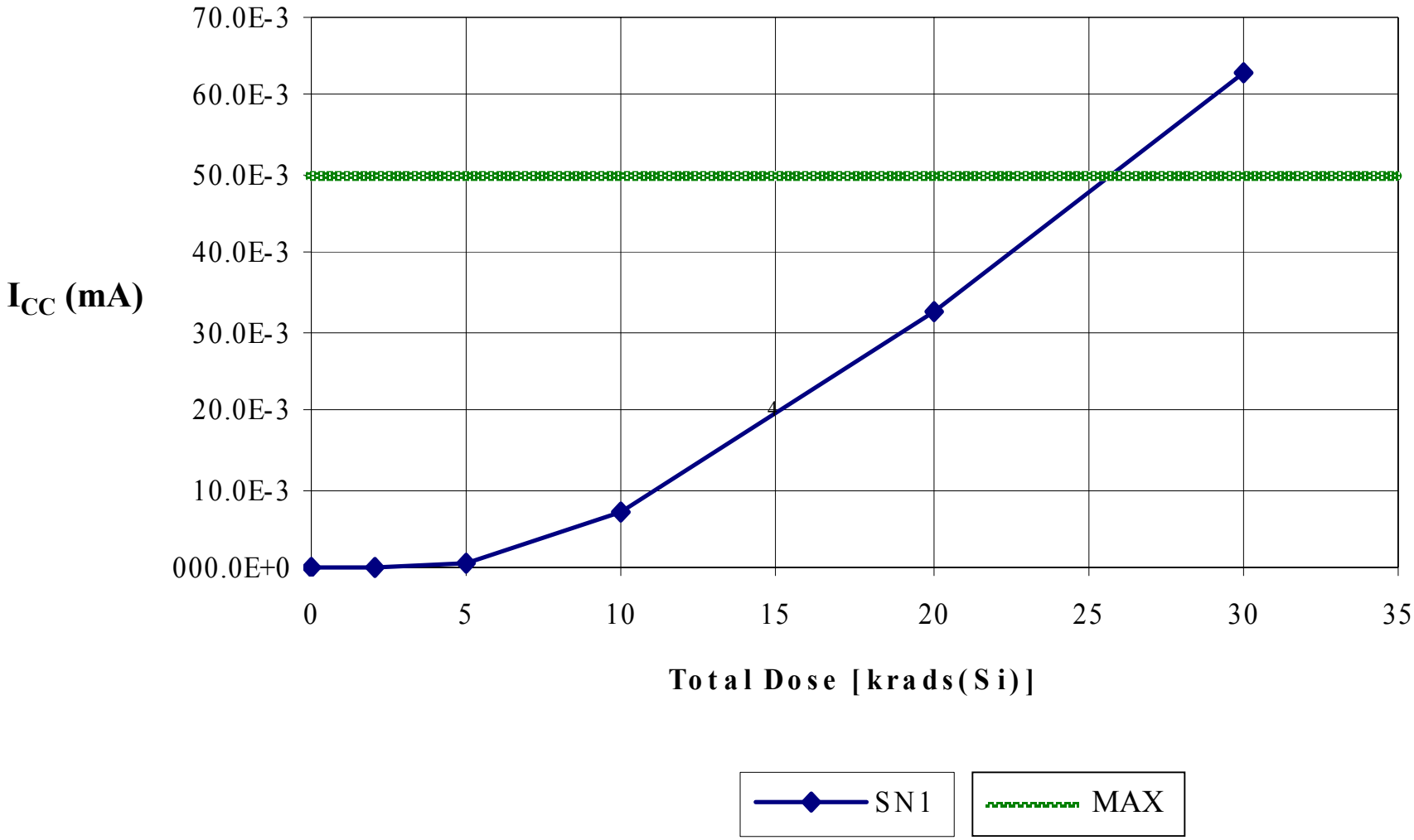
Co-60 TID Testing
I_{IL} vs. Total Dose



Co-60 TID Testing
I_{IH} vs. Total Dose



Co-60 TID Testing
I_{CC} vs. Total Dose



Co-60 TID Test Results

SEi's SF6 0.8µm CMOS gate array process demonstrated intrinsic total dose hardness up to 25 krad (Si).

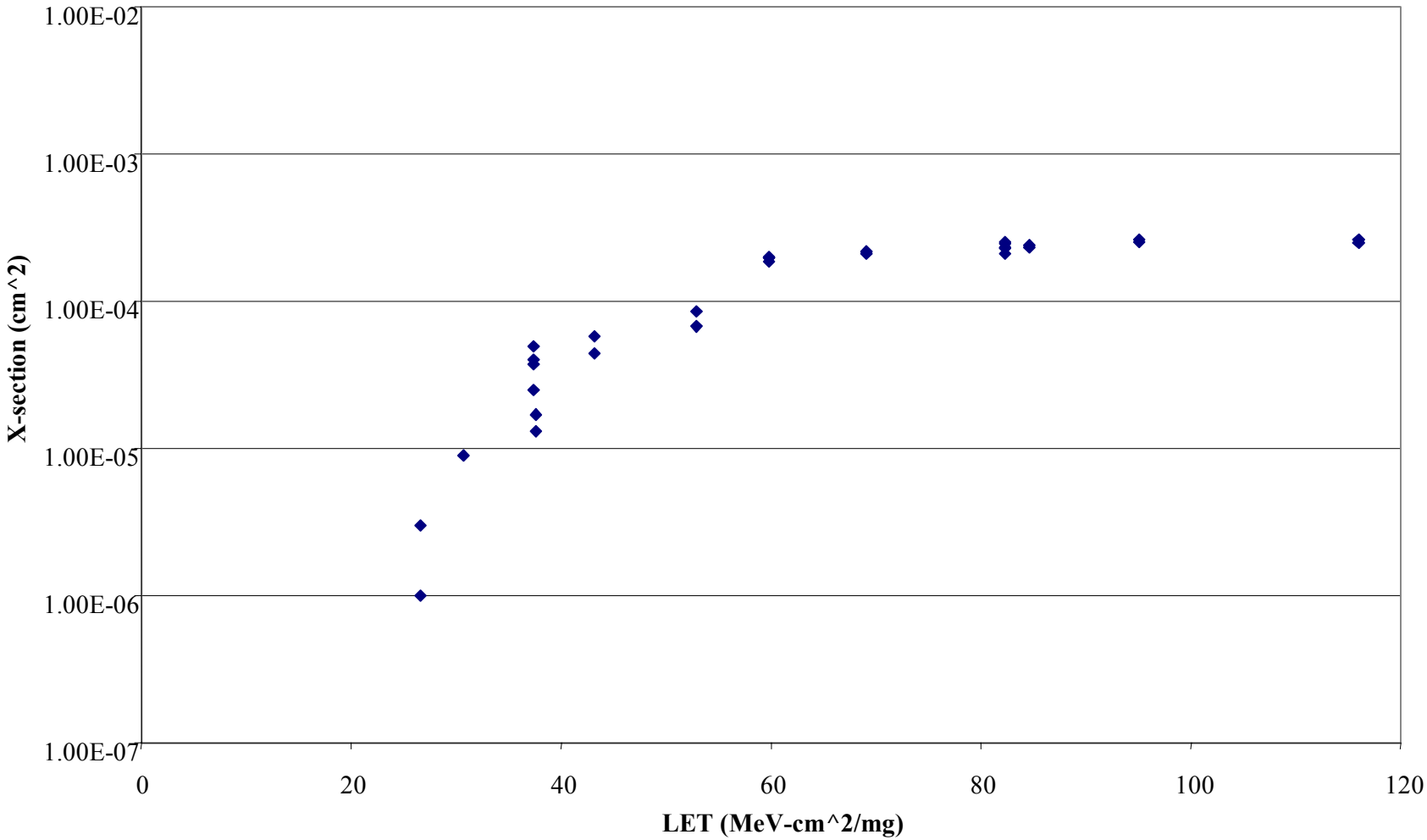
Results of intrinsic total dose testing combined with SEi's knowledge of space radiation environments, RAD-PAK® packaging shielding technology, and mission dependent requirements indicate the possibility of enhanced total dose hardness greater than 100 krad(Si).

Heavy Ion SEE Testing

- Heavy ion SEE testing was performed using the Brookhaven National Laboratory (BNL) Tandem Van De Graaff generator.
- Five different ions were selected (Br, I, Au, Cl and Ni) and used at angles from normal incidence to a maximum of 45° (maximum effective LET = 116 MeV/mg/cm^2).
- Fluence for each run = 10^6 ions/cm^2.
- Device modules containing combinatorial and sequential logic were tested.
- No single event latchups were observed on any of the devices
- No single event upsets were detected in the combinatorial logic gates.
- Figure 1 shows the SEU response for the flip-flop logic gates.
- Onset of flip-flop errors were observed at approximately 26 MeV/mg/cm^2 and a saturated cross section of 1.7 x 10^{-6} cm^2/bit.

Heavy Ion SEU Results

Figure 1. SF6 SEU Device Cross-Section vs. LET

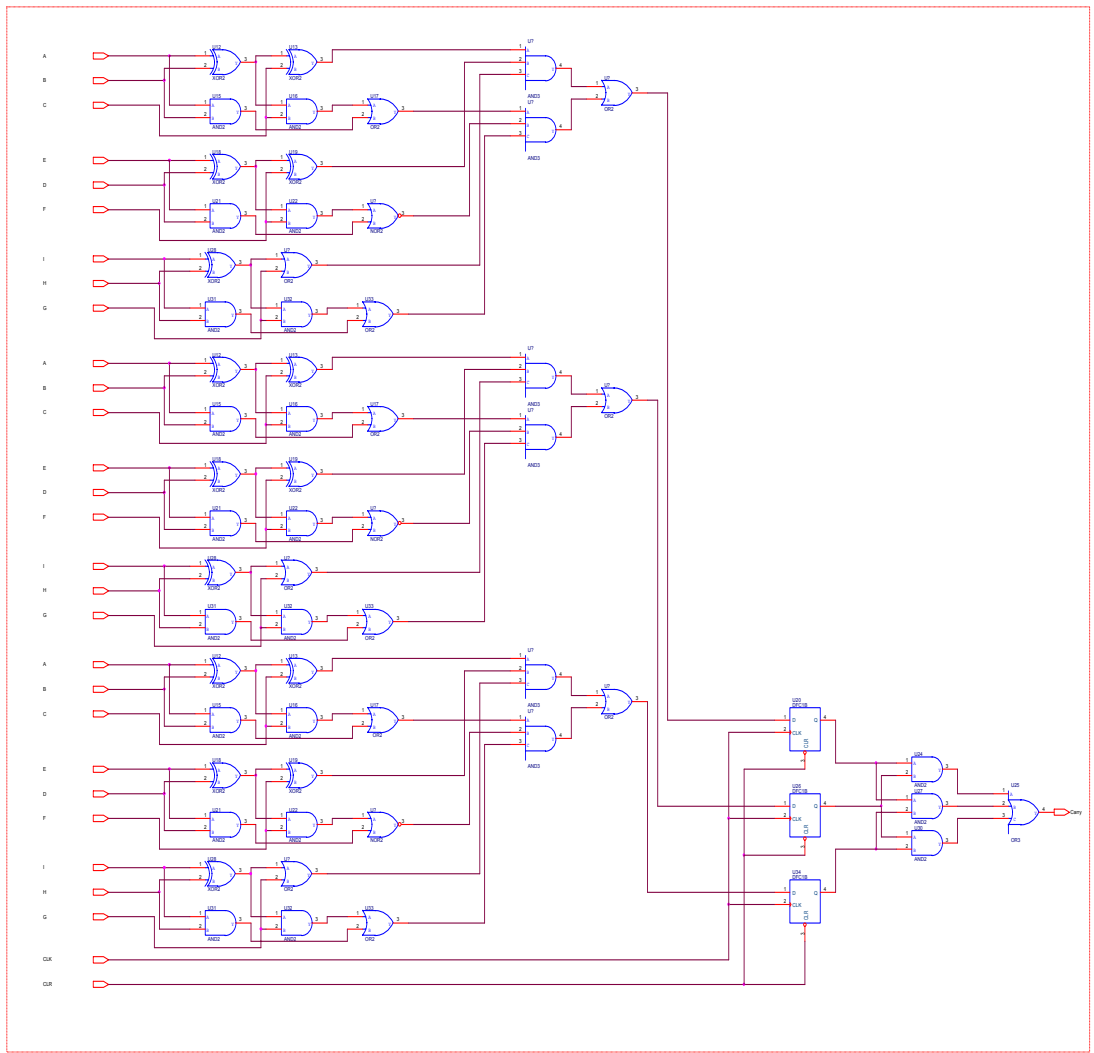


What is SEi's SEMD™ Technology

- SEMD™ methodology is a modified triple module redundancy (TMR) voting scheme which dramatically reduces SEU flip-flop errors.
- The upset error rate (90% worst case, geosynchronous orbit) improves from approximately 3 x 10^{-7} errors/bit-day without SEMD™ to better than 1 x 10^{-10} errors/bit-day with SEMD™.
- SEMD™ requires less gate usage to implement and produce designs that are more resistant to SEU effects than traditional TMR design techniques.
- Figures 2 and 3 illustrate the SEMD™ gate usage advantage.

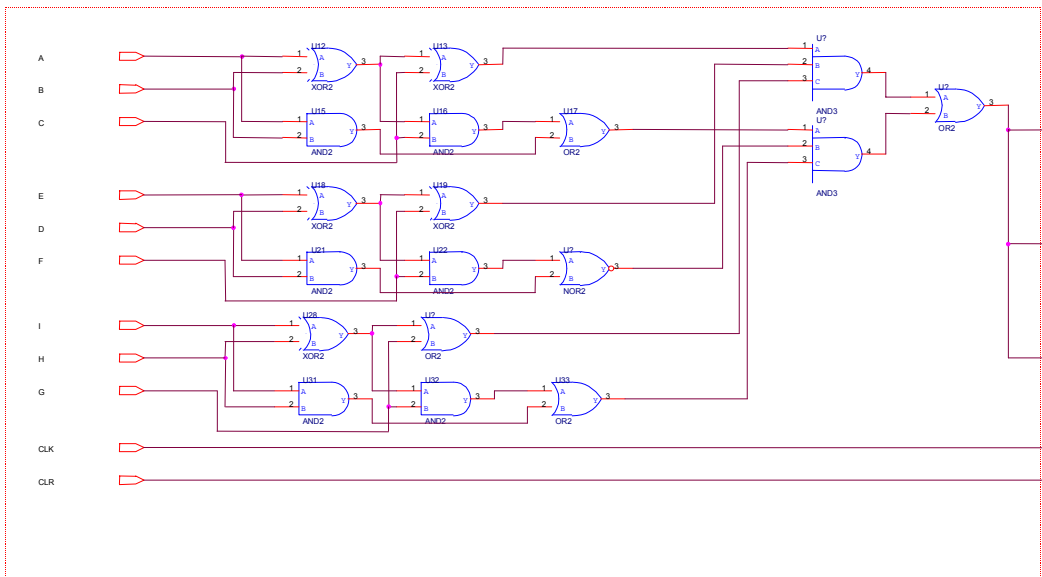
Combinatorial Logic using Traditional TMR

Figure 2

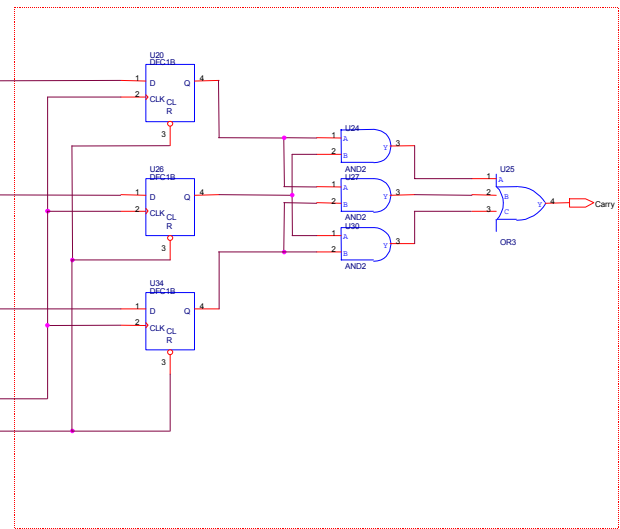


Combinatorial Logic Coupled with SEMD™

Figure 3



SEI's FAB6 SEE-Immuned Combinatorial



Triple Modular Redundant (TMR) voting dramaticly reduces SEU.

Summary

- SEi's commercial SF6 0.8µm gate array process passed MIL-STD-883, Method 1019 total dose requirements at 25 krad(Si) at a dose rate of ~10 rad/sec.
- Results of intrinsic total dose testing combined with SEi's RAD-PAK® packaging shielding technology indicate the possibility of enhanced total dose hardness greater than 100 krad(Si).
- The SF6 gate arrays are SEL immune to an LET of 116 MeV/mg/cm^2.
- Using SEi's SEU-hardened SEMD™ methodology, single event error rates less than 1 x 10^{-10} errors/bit-day can be achieved.